ESE 555: Advanced VLSI System Design **Fall 2011**

Instructor: Emre Salman
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Office: Room 257, Light Engineering Building
Office hours: Tuesdays 10 am to 12 pm and Thursdays 4 pm to 6 pm

Course Description:

This course describes the well established integrated circuit design process. VLSI circuit design techniques in the MOS technology are presented. Topics include MOS transistor theory, CMOS processing technology, VLSI design methodologies, MOS digital circuit analysis and various CMOS circuit design techniques. Integrated digital systems are designed and simulated throughout the course using VLSI design tools. At the end of the course, students will understand and experience the conventional VLSI design flow, and gain sufficient background for more advanced courses in the field.

Course Requirements:

There will be several computer-aided design and analysis assignments throughout the course. The students are also expected to complete a design project (schematic and layout) using Cadence IC design tools.

Prerequisite:

BSc in electrical engineering/computer engineering or computer science. Undergraduate students: ESE 330 and ESE 355.

Teaching Material:

Required

- N. Weste and D. Harris CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition, Addison Wesley

Recommended

- R. Jacob Baker CMOS Circuit Design, Layout, and Simulation, 3rd edition Wiley-IEEE Press 0470881321
- Erik Brunvand Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, 1st edition Addison Wesley

Course Content: Course consists of the following subjects

- Introduction and motivation
- Design flow and summary of VLSI design methodologies
- CMOS fabrication flow
- Transistor theory and transistor nonidealities
- Scaling theory

- Power/energy and low power design techniques
- SPICE/Circuit analysis and simulation techniques
- Combinational circuit design and circuit families
- Sequential circuit design
- Adders and datapaths
- Memory design
- Introduction to interconnects
- Packaging, power, and clock
- CMOS reliability
- Design for testability
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Grading:

- Midterm: 25%
- CAD assignments 30%
- Final project and report written in *IEEE* format: 45%

If you have a physical, psychological, medical or learning disability that may impact on your ability to carry out assigned course work, you are urged to contact the staff in the Disabled Student Services office (DSS), Room 133, Humanities, 632-6748/TDD. DSS will review your concerns and determine, with you, what accommodations are necessary and appropriate.